IN THE CLAIMS

1. – 13 Cancelled.

14. (Currently amended) A power semiconductor device with trench gates comprising:

a semiconductor substrate;

a source layer at one surface of the substrate and comprising a high concentration of a dopant of one polarity;

a well layer beneath the source layer doped with a dopant of opposite polarity;

a plurality of trenches penetrating the source layer, said trenches substantially filled with conductive material;

a highly conductive layer on the surface of the source layer comprising a material reacted from a metal and the semiconductor substrate;

an insulating layer on the highly conductive layer;

vias formed in the insulating layer and extending to the highly conductive layer on the source layer;

conductive material filling the vias for contacting the highly conductive layer.

15. – 19. Cancelled.

20. (New) The power semiconductor device of claim 14 wherein the trenches are filled with polysilicon and the top surface of the polysilicon is covered with a highly conductive material reacted from a metal and the polysilicon.

21. (New) The power semiconductor device of claim 14 wherein the highly conductive layer is a silicide.

22. (New) The power semiconductor device of claim 21 wherein the highly conductive layer is a silicide.

23. (New) The power semiconductor device of claim 22 or 23 wherein the silicide is reacted from platinum or titanium.

24. (New) The power semiconductor device of claim 14 wherein the insulating material on the highly conductive source layer is BPSG, PSG, silicon dioxide or silicon nitride.

25. (New) The power semiconductor device of claim 14 wherein the trenches are lined with a trench wall insulating material and the insulating material on the highly conductive source layer contacts the ends of the trench wall insulating layer lining the walls of the trenches.

26. (New) The power semiconductor device of claim 14 wherein one or more vias terminated on the surface of the highly conductive source layer for making electrical contact between the highly conductive source layer and the conductive material filling the via(s).